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10/523,031	02/02/2005	Daniel Shane O'Sullivan	4403-40000US6	8713

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EXAMINER	
FAHERTY, COREY S	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
09/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/523,031	O'SULLIVAN, DANIEL SHANE	
	Examiner	Art Unit	
	Corey S. Faherty	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *144,145,155-158,160,164,165,167-172 and 1615* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *144,145,155-158,160,164,165,167-172 and 1615* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the reply filed on 09/04/2007.

2. Claims 144-145, 155-158, 160, 164-165, 167-172 and 1615 are pending in the application and have been examined.

Specification

3. The title has been amended to more specifically state the invention. The objection to the specification is therefore withdrawn.

Drawings

4. New drawings 1A, 1B, 3 and 4 have been received and are accepted.

5. The drawings are objected to because the text on them is illegible. For instance, the text on Figures 2 and 5-30 is not clear enough to be easily read. Applicant is required to submit new drawings such that all text is clear enough to be read easily. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. Claims 156 and 168-170 have been amended to clarify their scope. The U.S.C. 112, second paragraph rejections of these claims made in the previous office action are therefore withdrawn.

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 144-145, 155-158, 160, 164-165, 167-172 and 1615 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Claims 144 and 1615 contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), *at the time the application was filed*, had possession of the claimed invention. The examiner is unable to locate the new subject matter in the original disclosure and applicant has failed to provide any evidence of such disclosure.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 144-145, 155-158, 160, 164-165 and 167-172 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 144 recites the limitation "the processing resource of the first type" in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 144, 155-156, 164-165, 167-170 and 1615 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonola (U.S. Patent 5,706,514) in view of Bridges et al. (U.S. Patent 6,081,860), referenced from here forward as Bridges.

15. Regarding claim 144, Bonola discloses a method of execution-instruction delegation between processing resources of at least two different types [abstract], comprising: obtaining an execution instruction, wherein the execution instruction is obtained at a processing resource of a first type [col. 3, line 26; a command is encountered by a host, or master, processor]; determining whether an operation-code within the execution instruction should be delegated to an other processing resource [col. 3, lines 25-29; it is determined if the instruction is of a type that cannot be executed by the host processor] of a second type different from the first type [col. 3, lines 36-51; when an encountered instruction is of a type that cannot currently be executed by the host processor, the host processor transfers data to a slave processor's registers so that the slave processor may execute the instruction]; executing the execution instruction with the processing resource of the first type, if the operation-code within the execution instruction should not be delegated to the other processing resource [col. 3, lines 23-44; if the encountered instruction is not of a type that cannot currently be executed by the host processor, the host processor continues executing it normally]; and routing the execution instruction to the other processing resource, if the operation-code within the execution instruction is for the other processing resource [col. 3, lines 36-51; when an encountered instruction is of a type that cannot currently be executed by the host processor, the host processor transfers data to a slave processor's registers so that the slave processor may execute the instruction].

Bonola does not explicitly disclose that the system has multiple host, or master, processors each of which delegates instructions to a single slave processor. However, Bonola does teach that other arrangements of multiprocessor computer systems could be used for carrying out the invention [col. 7, lines 11-15]. Bridges discloses such an alternate arrangement

for a multiprocessor system having multiple master processors and multiple slave processors [Fig. 1]. Bridges further discloses that multiple master processors issue requests to a slave processor [col. 6, lines 33-36]. Such a system allows for any of the master processors to gain the benefit of having a slave processor. It therefore would have been obvious to a person of ordinary skill in the art at the time the invention was made to have multiple host, or master, processors delegate instruction requests to a slave processor in the system of Bonola because Bridges teaches such a multiprocessor system for handling master processor requests.

16. Regarding claim 155, Bonola in view of Bridges discloses the method of claim 144, wherein the operation-code indicates a type of resource on which to execute [Bonola, col. 3, lines 25-30; an instruction specifies a certain mode of processor on which it can executed].

17. Regarding claim 156, Bonola in view of Bridges discloses the method of claim 144, wherein the other processing resource may be the originating processing resource [Bonola, col. 3, lines 23-44; if the encountered instruction is not of a type that cannot currently be executed by the host processor, the host processor continues executing it normally].

18. Regarding claim 164, Bonola in view of Bridges discloses the method of claim 144, wherein a processing resource is an execution-instruction processing cache [Bonola, col. 3, lines 37-42; the slave processor's registers are used to temporarily hold all data that is necessary for the slave processor to perform the execution provided to it by the host processor].

19. Regarding claim 165, Bonola in view of Bridges discloses the method of claim 144, wherein routing occurs through an execution-instruction signal router [Bonola, col. 3, lines 37-42; the slave processor's registers are used to temporarily hold all data that is necessary for the slave processor to perform the execution provided to it by the host processor; Fig. 1; col. 4, lines

43-45; a host bus is also provided to allow the host processor to communicate with the slave processors].

20. Regarding claims 167 and 1615, Bonola in view of Bridges discloses the method of claim 144, wherein a processing resource may sleep while an other processing resource executes delegated execution-instructions [Bonola, col. 8, lines 55-61; col. 9, lines 64-66; a slave processor may enter a sleep mode while the host processor or other slave processors execute instructions].

21. Regarding claim 168, Bonola in view of Bridges discloses the method of claim 144, wherein the execution-instruction signal causes various processing resources dynamically to turn on and off [Bonola, col. 8, lines 55-61; col. 9, lines 64-66; slave processors may enter a sleep mode in which they do not execute instructions].

22. Regarding claim 169, Bonola in view of Bridges discloses the method of claim 144, wherein the execution-instruction signal from processing resources themselves shuts off processing resources while idling [Bonola, col. 8, lines 55-61; col. 9, lines 64-66; slave processors may enter a sleep mode in which they do not execute instructions].

23. Regarding claim 170, Bonola in view of Bridges discloses the method of claim 144, wherein the execution-instruction signal from processing resources themselves turn on processing resources when execution-instruction signal processing is required [Bonola, col. 8, lines 55-61; col. 9, lines 64-66; a slave processor may be removed from sleep mode when it is necessary for executing instructions that the host processor is unable to execute].

24. Claims 144, 171-172 and 1615 are rejected under 35 U.S.C. 102(e) as being anticipated by Butterworth et al. (U.S. Patent 6,907,454), referenced from here forward as Butterworth, in view of Bridges.

25. Regarding claims 144 and 1615, Butterworth discloses a method of execution-instruction delegation between processing resources of at least two different types [abstract], comprising: obtaining an execution instruction, wherein the execution instruction is obtained at a processing resource of a first type [col. 2, lines 48-50; a master processor receives a memory access instruction]; determining whether an operation-code within the execution instruction should be delegated to an other processing resource of a second type different from the first type [col. 2, lines 48-54; the master processor determines that an instruction is of a memory access type and, if it is, determines that it should be sent to a slave processor]; executing the execution instruction with the processing resource of the first type, if the operation-code within the execution instruction should not be delegated to the other processing resource [col. 2, lines 44-58; the master processor executes non-memory access instructions normally]; routing the execution instruction to the other processing resource, if the operation-code within the execution instruction is for the other processing resource [col. 2, lines 53-54; for memory access instructions, the master processor writes a request to the slave processor to carry out the instruction].

Butterworth does not explicitly disclose that the system has multiple master processors each of which delegates instructions to a single slave processor. Bridges discloses a multiprocessor system having multiple master processors and multiple slave processors [Fig. 1]. Bridges further discloses that multiple master processors issue requests to a slave processor [col.

6, lines 33-36]. Such a system allows for any of the master processors to gain the benefit of having a slave processor. It therefore would have been obvious to a person of ordinary skill in the art at the time the invention was made to have multiple master processors delegate instruction requests to a slave processor in the system of Butterworth because Bridges teaches such a multiprocessor system for handling master processor requests.

26. Regarding claim 171, Butterworth in view of Bridges discloses the method of claim 144, wherein processing resources are communicatively disposed on a same die [Butterworth, col. 4, lines 36-40; a bridge device for communication between the memory and the slave processor may be integrated into a single chip package with the slave processor].

27. Regarding claim 172, Butterworth in view of Bridges discloses the method of claim 171, wherein an execution-instruction signal router is on the same die with processing resources [Butterworth, col. 4, lines 36-40; a bridge device for communication between the memory and the slave processor may be integrated into a single chip package with the slave processor].

28. Claim 145 is rejected under 35 U.S.C. 103(a) as being unpatentable over Butterworth in view of Bridges as applied to claim 144 above.

29. Regarding claim 145, Butterworth discloses the method of claim 145, but does not explicitly disclose that the method is completed within a single processing cycle.

The purpose of the Butterworth design is to reduce the processing delay of a memory operation [col. 1, lines 59-65]. Instead of forcing a processor to incur all of the delay necessary for executing a memory operation, the processor instead delegates the operation to a second processor [col. 2, lines 44-58]. If the first processor is able to perform this delegation quickly, it can continue executing other instructions [col. 5, lines 50-51] while the second processor

performs the memory operation. The fewer clock cycles it takes for the first processor to perform the delegation, the more time the first processor will have to execute other instructions while the second processor is performing the memory operation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to complete the instruction-delegation method disclosed in Butterworth in a single processing cycle because doing so would allow the master processor to begin executing other instructions more quickly and thus execute more code overall while the slave processor is performing a memory operation.

30. Claims 157-158 and 160 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonola in view of Bridges as applied to claim 144 above, and further in view of Mohamed et al. (U.S. Patent 5,978,838), referenced from here forward as Mohamed.

31. Regarding claim 157, Bonola in view of Bridges does not explicitly disclose that a processing resource is an integer-processing unit.

Mohamed discloses a system similar to that of Bonola in which two processors interact to efficiently process instructions [col. 1, lines 61-67]. The system includes integer-processing units for executing integer instructions [col. 5, lines 8-15].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an integer-processing unit as a processing resource in the system of Bonola because Mohamed discloses doing including an integer-processing unit in a multi-processor system [col. 5, lines 8-15] and doing so allows the system to execute integer instructions. Furthermore, without an integer-processing unit, the system of Bonola would be unable to execute integer instructions, greatly limiting the amount of software that it could run.

32. Regarding claim 158, Bonola in view of Bridges does not explicitly disclose that a processing resource is a mathematical processing unit.

Mohamed discloses a system similar to that of Bonola in which two processors interact to efficiently process instructions [col. 1, lines 19-26]. The system includes a math co-processor [col. 1, line 24].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a mathematical processing unit as a processing resource in the system of Bonola because Mohamed discloses including a math processor in a multi-processor system [col. 1, lines 19-26] and doing so allows the system to more efficiently execute mathematical operations. The use of a mathematical processor as a slave processor in the system of Bonola allows the host processor to be designed for better execution of other types of instructions, allowing for greater overall processing efficiency. Furthermore, the addition of a mode in which a slave processor behaves a mathematical processor allows the system of Bonola to execute mathematical operations, also potentially increasing overall processing efficiency.

33. Regarding claim 160, Bonola in view of Bridges does not explicitly disclose that a processing resource is a vector-processing unit.

Mohamed discloses a system similar to that of Bonola in which two processors interact to efficiently process instructions [col. 1, lines 61-67]. The system includes a vector processor [abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a vector-processing unit as a processing resource in the system of Bonola because Mohamed discloses including a vector processor in a multi-processor system [abstract]

and doing so allows a system to more efficiently execute vector instructions without impacting the execution efficiency of a main processor. The addition of a vector processing mode to a slave processor in the system of Bonola would allow the host processor to delegate vector operations to slave processors while continuing to execute other instructions, resulting in greater processing efficiency.

Response to Arguments

34. Applicant's arguments filed 09/04/2007 have been fully considered but they are not persuasive.

35. Applicant's arguments with respect to claim 144 are moot in view of the new grounds of rejection.

36. Regarding claim 155, applicant alleges that Bonola does not disclose an operation code that indicates a type of resource on which to execute. More specifically, applicant argues that a processor mode in Bonola is not equivalent to a processor type as is claimed. The examiner respectfully disagrees on the grounds that applicant is using an unreasonably narrow interpretation of the word "type". A "type" of a processor may indicate virtually anything about that processor such its instruction set architecture, its manufacturer, or its current operating mode. Applicant's argument is therefore not persuasive.

37. Regarding claims 157, 158 and 160, applicant asserts that Bonola does not explicitly disclose an integer processing unit, a mathematical processing unit, or a vector-processing unit. The examiner does not disagree with these assertions, and notes that the previous office action explicitly stated these assertions in forming proper U.S.C. 103 rejections.

38. Regarding claim 164, applicant alleges that the slave registers of Bonola do not constitute an "execution-instruction processing cache" as recited in the claim, but fails to present any argument or evidence in support of this allegation. Furthermore, the slave registers of Bonola are used as a cache for data used in executing instructions [col. 3, lines 37-42], and thus clearly constitute an "execution-instruction processing cache". Applicant's argument is therefore not persuasive.

39. Regarding claim 145, applicant argues that it is doubtful that the system of Butterworth could be modified to perform the method of claim 144 in a single cycle. The examiner respectfully disagrees. To perform a logical operation in a single clock cycle, a system designer need only modify the processing frequency. Such modification is well known and common to a person of ordinary skill in the computer arts, and applicant's argument is therefore not persuasive. Furthermore, the number of clock cycles that it takes for an operation to complete is a design decision, and the benefits of completing an operation in a single clock cycle are well known in the computer arts.

40. Further regarding claims 157, 158 and 160, applicant alleges that Mohamed does not teach an integer processing unit, mathematical processing unit, or vector processing unit because those terms are further defined in the specification of the instant application, and Mohamed does not teach them as they are defined. To support this allegation, applicant states that these terms are further defined in "the Application at p. 12, and the specification generally." However, no explicit definitions for any of these terms can be found on page 12 of the specification, and generally referencing the specification does not constitute a proper citation for determining an explicit definition of a claimed term. Applicant's argument is therefore not persuasive.

Conclusion

41. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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